

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,847,248 B2
APPLICATION NO. : 10/043763
DATED : January 25, 2005
INVENTOR(S) : Ajit

Page 1 of 13

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page

(57) Abstract, line 1	Delete "input output", Insert --input/output--
(57) Abstract, line 3	Delete "so does", Insert --so do--

In the Claims

Column 10, line 47, Claim 3	Delete "not present", Insert --not present,--
Column 11, line 11, Claim 4	Delete "not present", Insert --not present,--
Column 11, line 28, Claim 5	Delete "not present", Insert --not present,--
Column 11, line 57, Claim 6	After "device", Insert --;--
Column 12, line 19, Claim 7	Delete "comprises"
Column 12, line 32, Claim 9	After "Semiconductor) ", Insert --device--

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,847,248 B2
APPLICATION NO. : 10/043763
DATED : January 25, 2005
INVENTOR(S) : Ajit

Page 2 of 13

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Drawings

FIG. 4, Sheet 4 of 23	Delete Drawing Sheet 4 and substitute therefore the Drawing Sheet, consisting of Fig. 4, as shown on the attached page
FIG. 6, Sheet 6 of 23	Delete Drawing Sheet 6 and substitute therefore the Drawing Sheet, consisting of Fig. 6, as shown on the attached page
FIG. 9A, Sheet 9 of 23	Delete Drawing Sheet 9 and substitute therefore the Drawing Sheet, consisting of Fig. 9A,, as shown on the attached page
FIG. 10, Sheet 11 of 23	Delete Drawing Sheet 11 and substitute therefore the Drawing Sheet, consisting of Fig. 10, as shown on the attached page
FIG. 11A, Sheet 12 of 23	Delete Drawing Sheet 12 and substitute therefore the Drawing Sheet, consisting of Fig. 11A, as shown on the attached page
FIG. 12A, Sheet 16 of 23	Delete Drawing Sheet 16 and substitute therefore the Drawing Sheet, consisting of Fig. 12A, as shown on the attached page

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,847,248 B2
APPLICATION NO. : 10/043763
DATED : January 25, 2005
INVENTOR(S) : Ajit

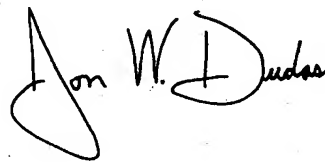
Page 3 of 13

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

FIG. 12B, Sheet 17 of 23	Delete Drawing Sheet 17 and substitute therefore the Drawing Sheet, consisting of Fig. 12B, as shown on the attached page
FIG. 13, Sheet 18 of 23	Delete Drawing Sheet 18 and substitute therefore the Drawing Sheet, consisting of Fig. 13, as shown on the attached page
FIG. 14, Sheet 19 of 23	Delete Drawing Sheet 19 and substitute therefore the Drawing Sheet, consisting of Fig. 14, as shown on the attached page
FIG. 18, Sheet 23 of 23	Delete Drawing Sheet 23 and substitute therefore the Drawing Sheet, consisting of Fig. 18, as shown on the attached page

Signed and Sealed this

Twenty-first Day of November, 2006

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looping initial "J" and a distinct "D".

JON W. DUDAS
Director of the United States Patent and Trademark Office

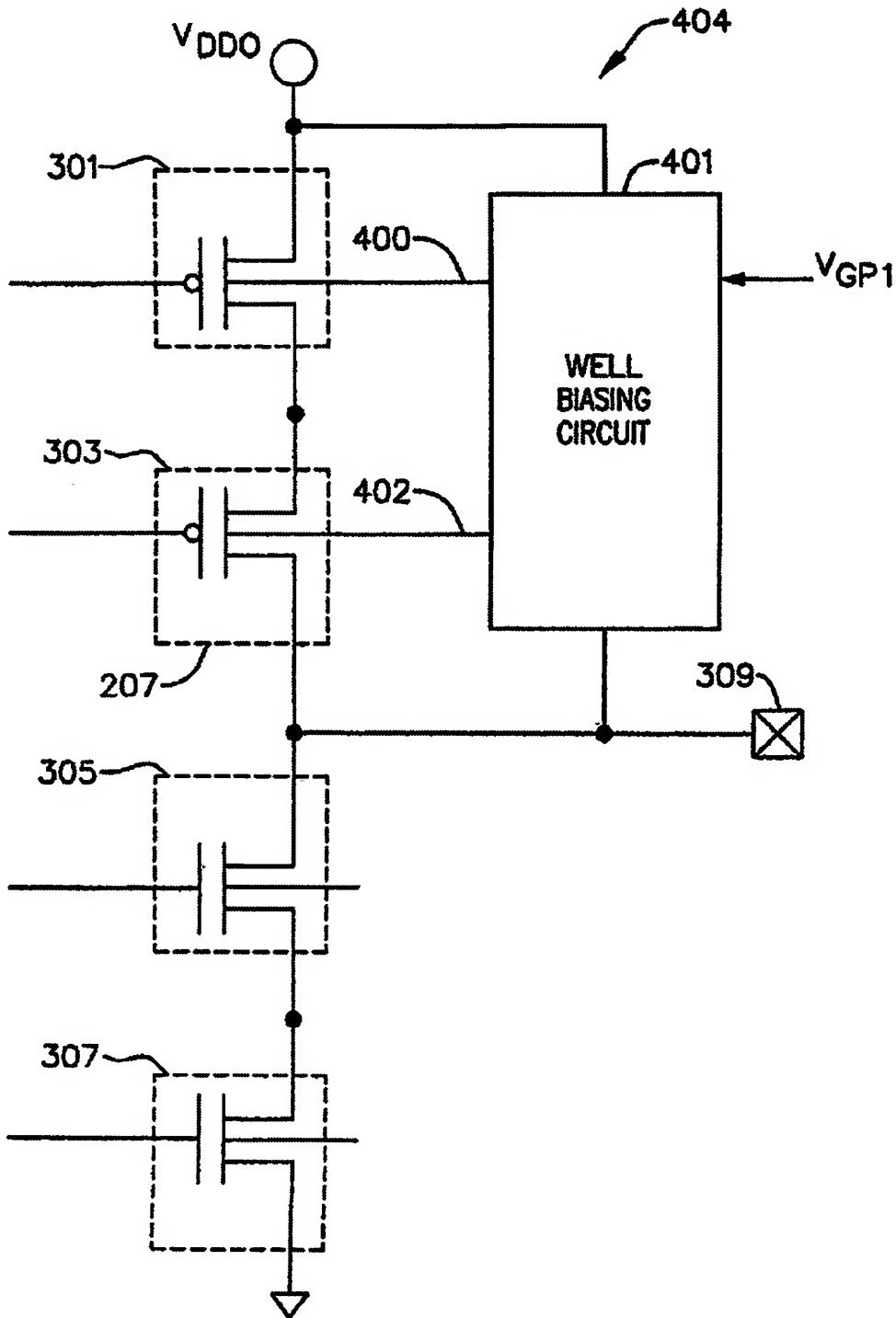
FIG. 4

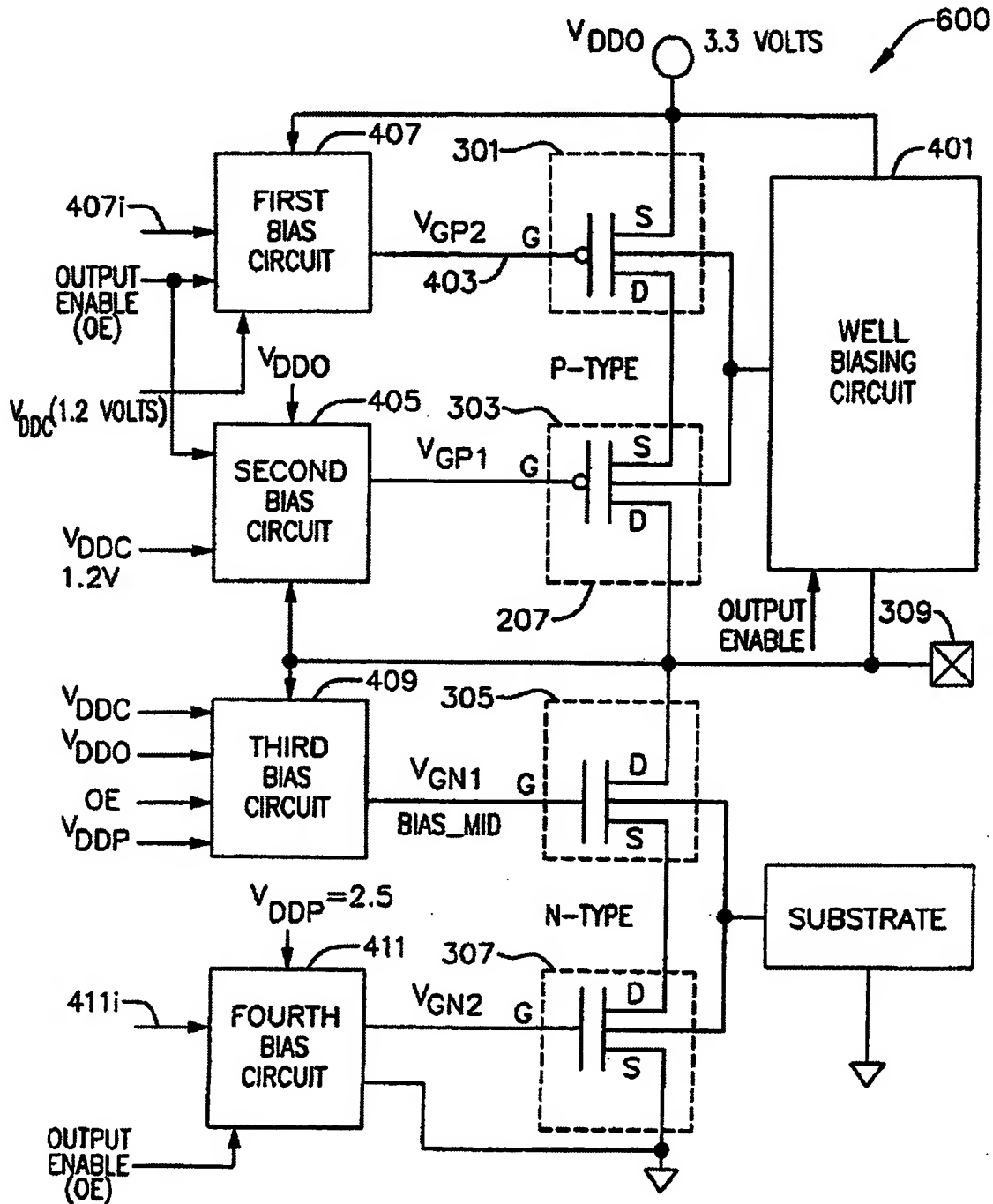
FIG. 6

FIG. 9A

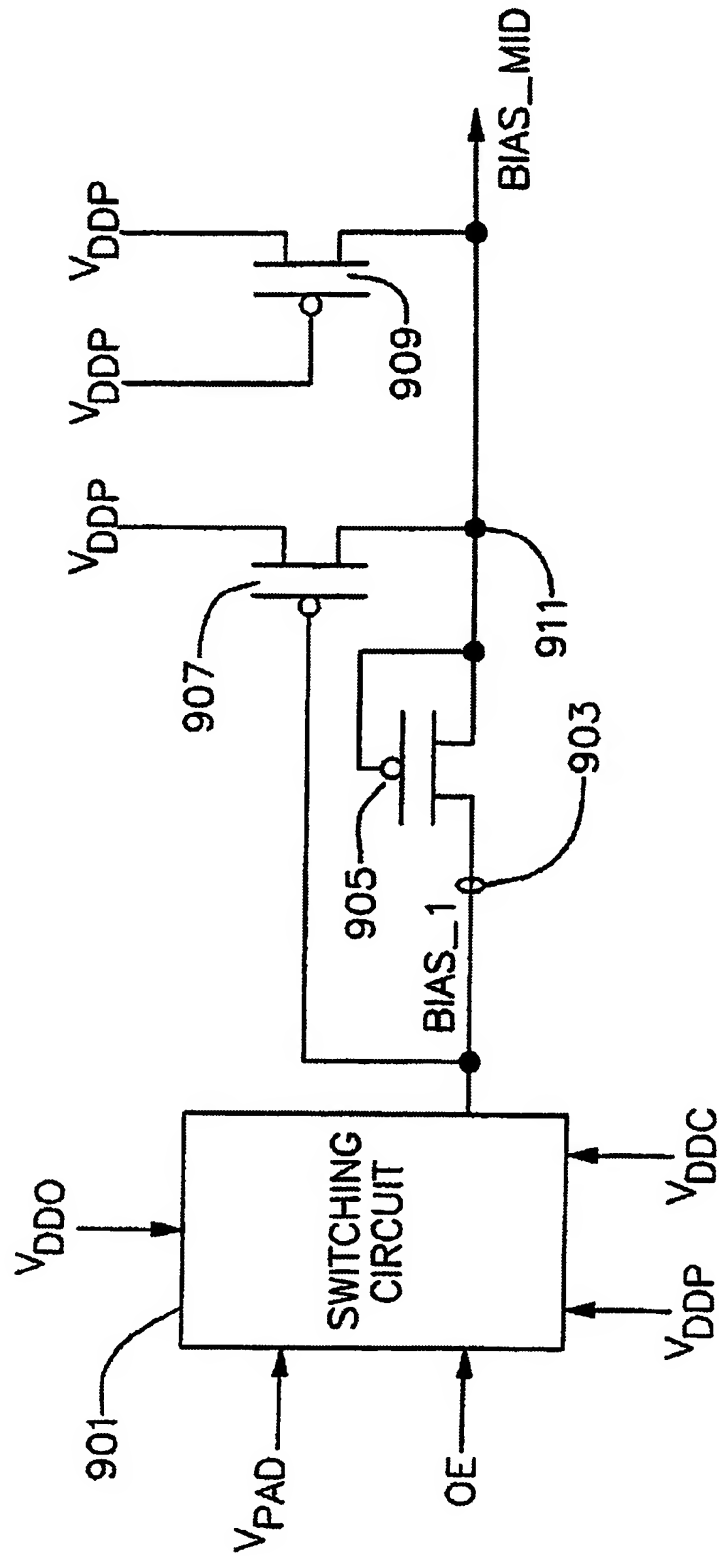


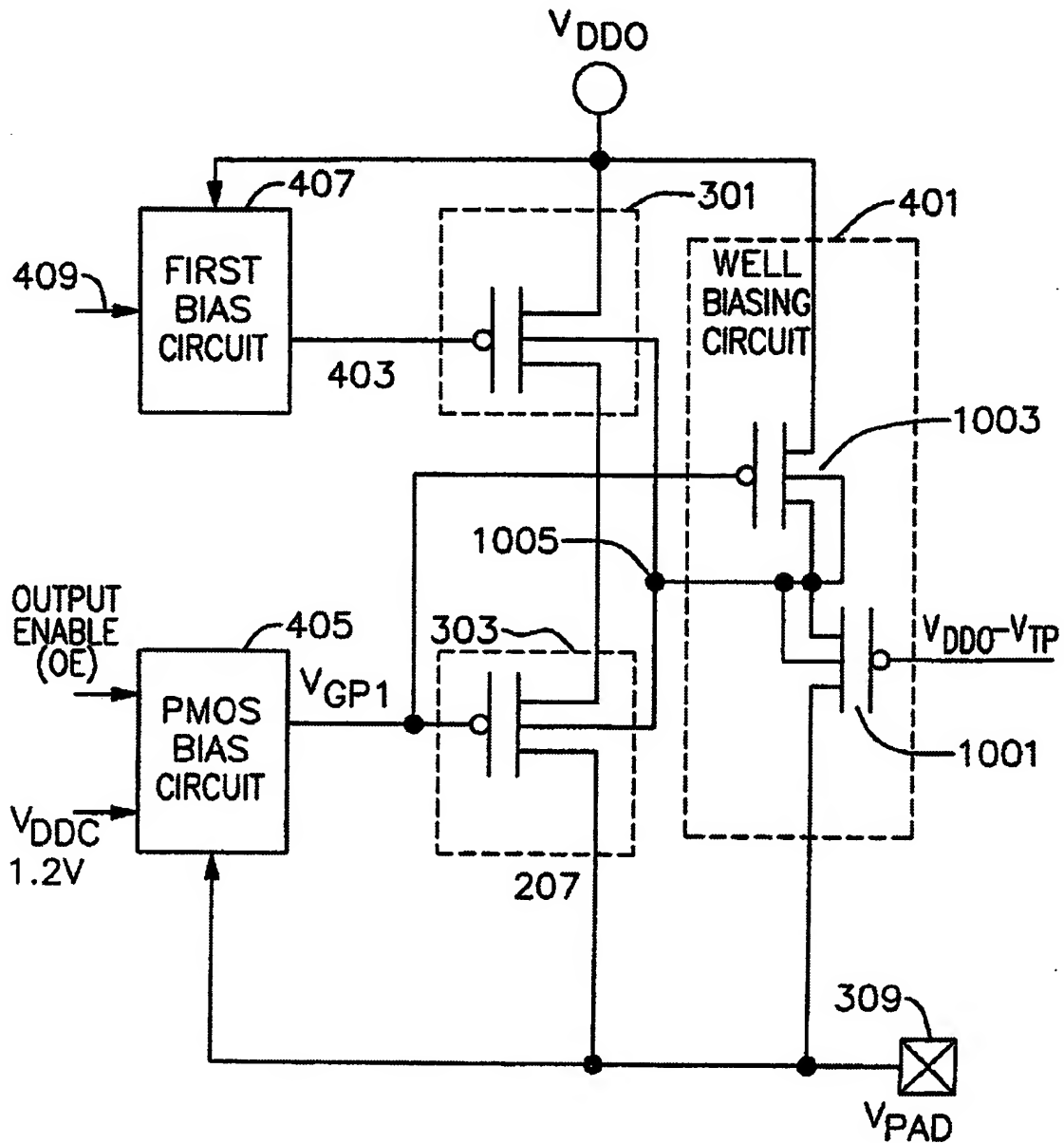
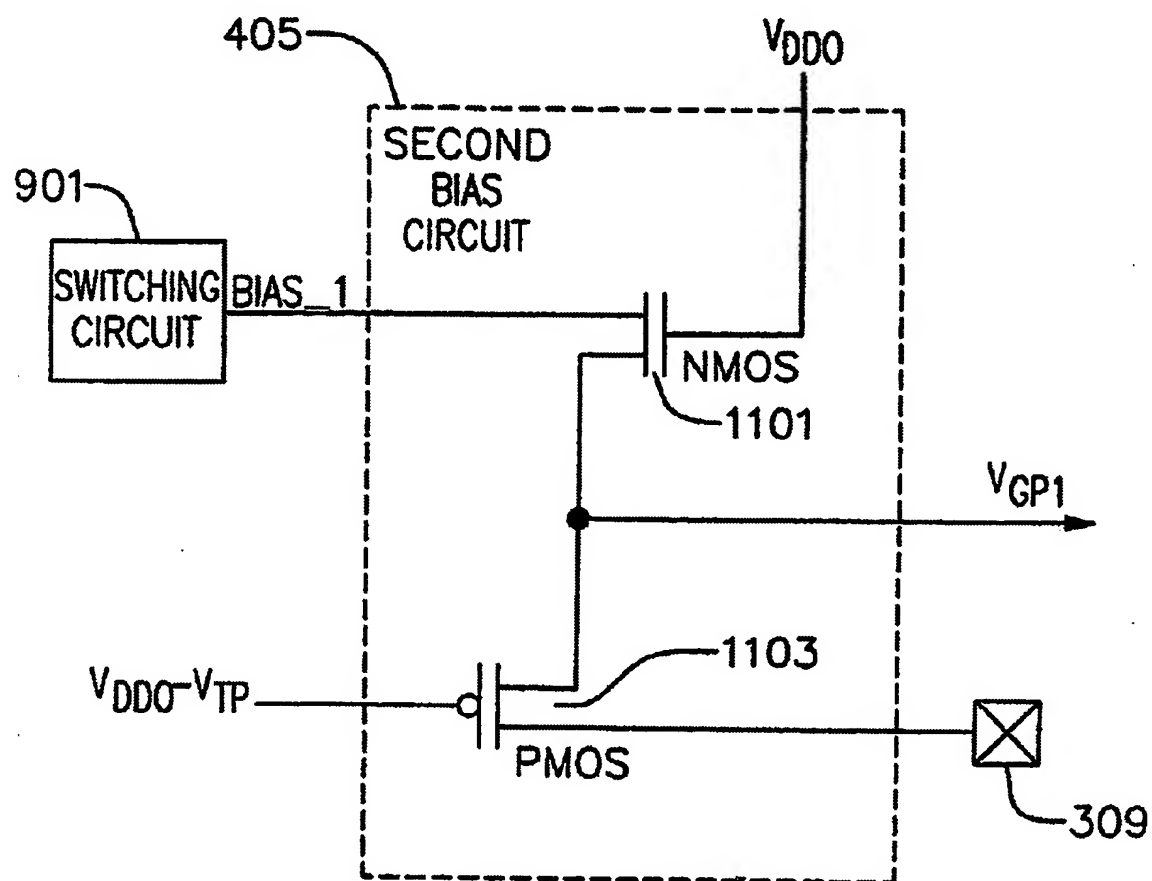
FIG. 10

FIG. 11A

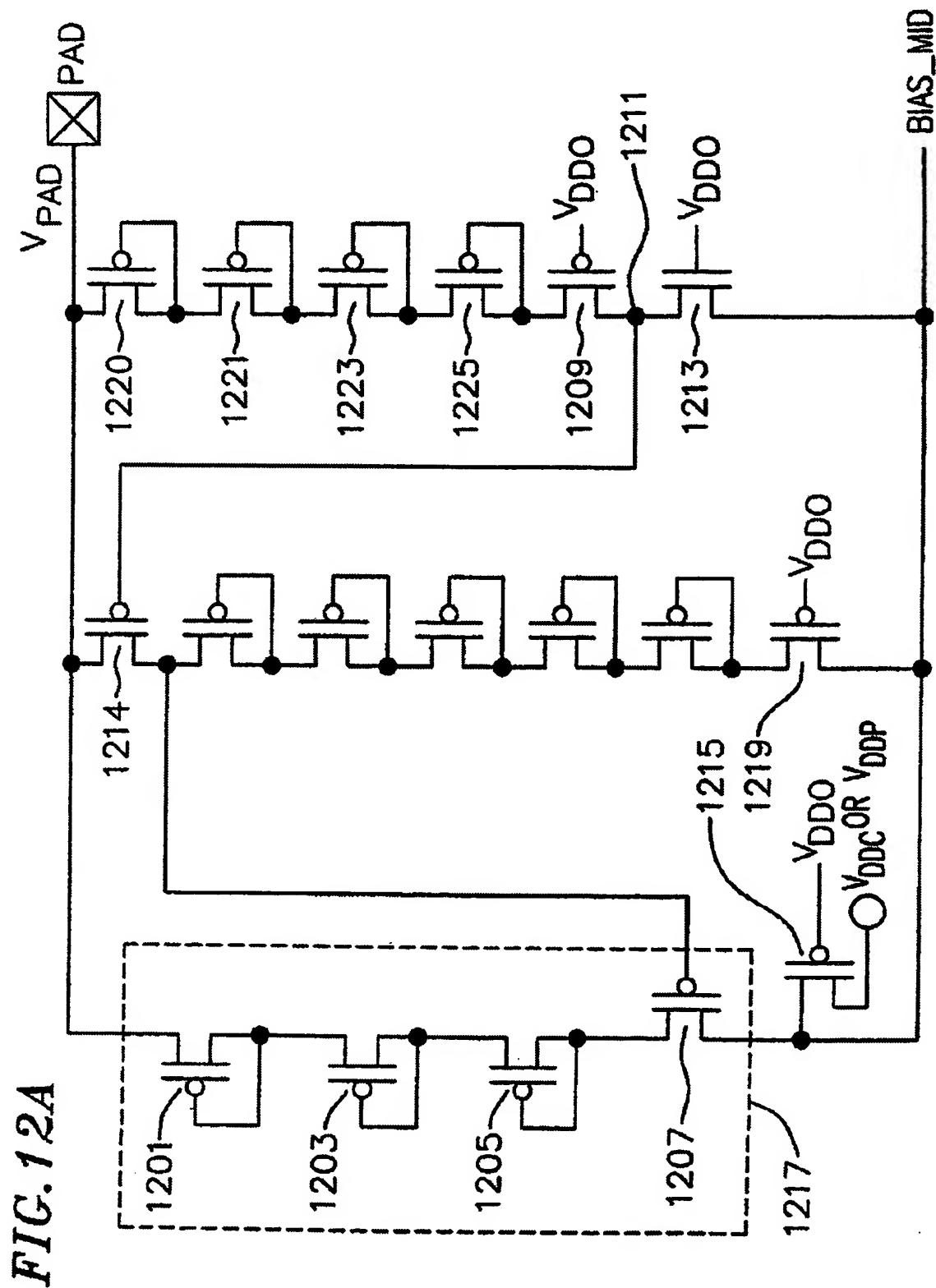


FIG. 12B

FIG. 12B is a circuit diagram of a multi-bit DAC. The circuit features a stack of PMOS transistors (1201, 1203, 1205, 1207, 1214, 1220, 1221, 1223, 1225, 1209, 1211, 1213, 1219) and NMOS transistors (1220, 1221, 1223, 1225, 1209, 1211, 1213, 1219). The PMOS transistors are connected to a PAD node (V_{PAD}) and a BIAS_MID node. The NMOS transistors are connected to a BIAS_MID node and a node B, which is also labeled V_{SSC} OR V_{DDC} OR V_{DDP} and 1255. A dashed box 1217 encloses transistors 1201, 1203, 1205, and 1207. The circuit is connected to a PAD node (V_{PAD}) and a BIAS_MID node. The bottom stack of NMOS transistors (1251, 1252, 1253) is connected to node B, which is also labeled V_{SSC} OR V_{DDC} OR V_{DDP} and 1255.

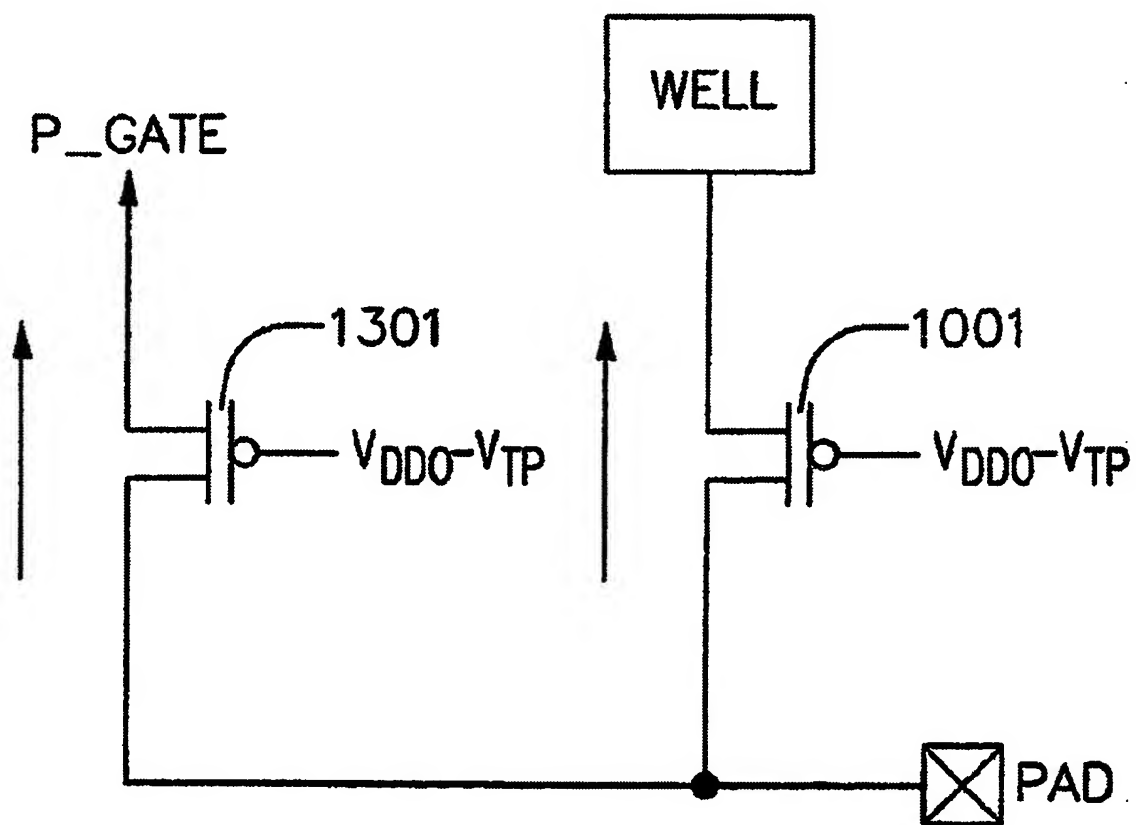
FIG. 13

FIG. 14

